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BEAM TEST OF A PROTOTYPE READ-OUT SYSTEM FOR PRECISION TRACKING DETECTORS AT LHC

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Abstract

A prototype of a read-out system developed for high spatial precision tracking detectors at LHC has been tested in a beam at CERN. It is based on a radiation hard CMOS front end chip which includes signal amplification, storage in an analogue delay line and a deconvolution filter. Data were transferred from the front end chip using an analogue fibre optic link employing a novel reflective electro-optic modulator and continuous laser light source remote from the detector. This is the first time such a system has been used in an experimental environment and is the basis of the system proposed for the CMS experiment at LHC.

1. Introduction

The read-out of high spatial precision tracking detectors, such as silicon or gas microstrips, in experiments at the CERN Large Hadron Collider (LHC) presents major challenges. The high density and large number of read-out channels imposes low power front end electronics, while the intrinsic sensitivity of the detectors requires low noise levels to be maintained throughout the operating lifetime of the experiments. This has to be achieved at bunch crossing rates of 40 MHz, with high fluxes of secondary particles giving rise to radiation levels not encountered before in particle physics experiments [1,2]. Typical levels are in the range 10 Mrad and 10^{14} particles.cm^{-2} over several years of operation.

To enable the reconstruction of charged particle tracks in the experiment, it is essential that each particle crossing the tracking layers is identified with good timing precision. In the case of silicon microstrip detectors the charge collection times are such that association of a signal to a single bunch crossing is achievable even after significant levels of radiation damage to the detectors. Microstrip gas detectors (MSGCs) are intrinsically slower because of the relatively thick detector layers required to generate reasonable ionisation signals and the achievable timing precision will be dominated by fluctuations in the density of primary ionisation. Nevertheless it is anticipated that, with appropriate electronics, events should be allocated to one of two bunch crossings in most cases.

Radiation damage to the detectors is still a cause for concern. Considerable progress has been made in the last few years in establishing limits to operation of both gas and semiconductor detectors. However, until recently, there was little experience with radiation hardened electronics technology and few possibilities to produce custom analogue circuits to instrument large systems of microstrip detectors. Several development programmes in Europe and in the USA have been designing and evaluating appropriate circuits and fabrication processes. One promising solution is CMOS technology because of previous experience in high energy physics, including low noise amplifiers for silicon strip read-out, and radiation hard CMOS processes were known to exist.

A front end electronics read-out chain for LHC has been developed by the RD20 collaboration [3,4]. The three essential elements of the signal processing system are:

- a charge sensitive preamplifier and shaper, providing low noise amplification with low power consumption,
- an analogue pipeline memory stage, providing a 3-4 μs level 1 trigger delay,
- an analogue signal processor, responsible for the timing accuracy.

The first radiation hard version of this system has been produced as a 32 channel chip using the Harris [5] 1.2μm CMOS AVLSIRA process where previous measurements have established the performance and radiation hardness at the transistor level[6].

An important goal of the RD20 architecture was to provide analogue data read-out. There are several potential advantages in analogue read-out, for example robustness against common mode noise in the system. In view of the requirement to operate with minimum power it is desirable to avoid analogue to digital conversion within the detector volume. It is also desirable to transfer the data from the tracking detector volume at high rate with the use of minimal material and extra noise. Optical fibre technology provides a means to achieve these aims and another LHC development project, RD23, has been investigating the potential of analogue data transfer based on electro-optic devices where a modulator reflectivity is varied in response to an applied voltage [7,8,9]. Significant progress has been made in demonstrating the potential of

this approach in laboratory evaluations and, in this test, this means of data transfer was used for the first time in an experimental environment.

The results reported here concern the first demonstration of a modest working system using the radiation hard analogue front end chip to read out signals from a silicon microstrip detector in a particle beam. The data were transferred by optical fibre using a 4 channel reflective modulator device to a counting room where digitisation and storage took place. The results have been compared with data transfer using coaxial cable, with some data taken simultaneously using both methods. This system forms the basis of the electronic read-out system proposed for the MSGC and silicon microstrip tracker of the CMS experiment at LHC [10].

2 Radiation hard front end electronics

The chip used in this test, the APV3, is a 32 channel radiation hard circuit produced using the Harris AVLSIRA 1.2μm bulk CMOS radiation hard process [5]. It will be succeeded by a 128 channel version (the APV5) which will also contain an integrated analogue multiplexer; this circuit is currently being fabricated [11]. In the tests described here the 32 outputs were multiplexed onto 4 lines using commercial integrated circuits.

The APV3 utilises the concept of slow shaping and stored sample deconvolution [3,4,12] using an amplifier and CR-RC filter with a time constant of 50 ns, an analogue pipeline, which samples the amplifier output voltage at the LHC beam crossing rate of 40 MHz, and an analogue pulse shape processor (APSP). The APSP effectively reshapes the amplifier output pulse to a form occupying one beam crossing interval, thus eliminating pileup. The pulse shape processing is carried out by forming a weighted sum of three consecutive temporal samples using a switched capacitor circuit. Deadtime and data loss are essentially non-existent because only events which have passed a first level trigger are processed. This may take up to 3.2μs for a decision and determines the required length of the pipeline.

2.1 APV3 architecture and design

The chip consists of 32 channels, each with 160 storage cells following the amplifier. Pointers control reading, writing and erasing of data within the pipeline array and a FIFO is used to store addresses of triggered columns. Data are read out through the signal processor where the output voltage levels can be sampled and held for read-out through an external analogue multiplexer. Data acquisition and read-out occur simultaneously. The sequencing of the pointers and signal processor are controlled using a standard cell logic block.

Figure 1 shows a functional schematic of the analogue front end. The preamplifier is a charge amplifier which produces a voltage step proportional to the input charge impulse and is the main source of noise within the circuit [6]. The charge to voltage gain ratio is determined by the feedback capacitor of 0.6 pF. The shaper is a close approximation to a CR-RC filter with additional gain. The nominal value of the time constant is 50 ns but is tuneable over a limited range using a voltage controlled input.

Each channel of analogue storage consists of an array of 160 switched capacitor elements. One side of the capacitor connects to a DC voltage level and the other to the write and read transistor switches. A third switch connects across the capacitor and is

used for erasing data. The output of the shaper is sampled every 25 ns and stored in the pipeline. An impulse is recovered by forming a weighted sum of several samples from successive time intervals; the method is explained in ref. [13]. Three samples are used, and if a signal occurs at time interval n, the voltage samples S_{n-1}, S_n and S_{n+1} are read from the pipeline when the chip is triggered (fig 2).
The analogue storage control logic (fig 3) is used to sequence the storage of analogue data within the capacitor array. Before data can be written into the array, the control logic must be initialised. Firstly, the FIFO, Skip Logic and Pointers are cleared by applying a RESET to the relevant inputs. Then, a token is passed to each of the pointers in order to start them up. The erase pointer is initialised first, followed one clock cycle later by the write pointer. In this prototype the trigger pointer is initialised after a fixed period of 128 clock cycles.

The pointers then shift along the analogue array maintaining the separations set up at initialisation. They are constructed so that, once initialised, they continuously loop around the array. When a trigger is received the column addressed by the trigger pointer is reserved for read-out by setting a flag in the skip logic and its address, generated by the encoder, is stored in the FIFO. Once a column has been triggered the pointers will jump over it on their next pass and will continue to skip the location until the sample stored there has been read out.

A switched capacitor filter, consisting of an amplifier and a switched capacitor network (fig 4), performs the deconvolution. The ratio of the capacitors $C_1 : C_2 : C_3$ is the same as the ratio of the weights required to deconvolute the signal $w_1 : w_2 : w_3$ [13] which for 25 ns sampling and 50 ns shaping time, requires weights of $w_1 = 0.446$, $w_2 = -1.472$, $w_3 = 1.213$. The APSP runs with four cycles of 1μs using a clock generated from the primary 40 MHz clock to the chip.

The three samples are read in sequence from the pipeline, and amplified onto the capacitors in the filter by switching r_{in1}, r_{in2} and r_{in3} in order. The three weighted samples are then summed by switching r_{out1} to connect the three capacitors in parallel at the input to the amplifier. Before each sample is read in, and before the sum is read out, the amplifier is reset by closing the reset switch. The summed value is then sampled and buffered at the output where it remains constant for 1μs. Since three samples are stored for each event, events which are less than three beam crossings apart would share the same storage. Reading samples from the pipeline into the APSP destroys the data which is held there, therefore a sample cannot be used twice from the same pipeline element and further triggers will be ignored for two cycles following a trigger.

A trigger and read-out control circuit controls the reset of the chip, generates trigger signals for the analogue storage array, and controls the APSP read-out. To increase flexibility and reduce design time, this block is constructed from standard cells. It carries out the following operations: initialisation of the erase, write, and trigger pointers, generation of global trigger and FIFO write clock, sequence retrieval of data from FIFO and enable decoder, sample & hold circuitry management and APSP read-out, buffering of clocks and reset to the analogue array control logic.

2.2 APV3 laboratory test results

Initial characterisation was carried out using a chip without detector attached and injecting test charges. Fig. 5 shows the response of the circuit loaded with several different input capacitance values to a signal corresponding to 24000e⁻. The pulse shape was virtually identical to the design and noise from the amplifier was measured, using

two additional channels on the chip for which the amplifier output was accessible, to be $ENC\ (e) = 550 + 50C_{load}(pF)$.

Fig. 6 illustrates a typical read-out sequence. The upper traces show two events, one with a signal present and the other without. The lower trace represents the difference between the two clearly indicating the presence of a signal which, for an injected charge of 32,000 electrons, gave an output voltage of 0.22V.

Fig. 7 shows the averaged deconvoluted output against signal injection time, which allows direct observation of the weighting function [13] of the filter. In comparison with the calculated cusp-like function the practical form of the weighting function has very little discontinuity at the peak and is almost gaussian in shape. The flattening of the peak is desirable, since the filter is less sensitive to errors in the phase of the clock relative to signal arrival time and also has a small but beneficial effect on the series noise of the system. Very little signal occurs beyond one clock cycle on either side of the maximum, demonstrating the effectiveness of the deconvolution technique.

Two problems have been identified with the APV3. A trivial error exists in the logic which mishandles two consecutive triggers which was overcome in operation by resetting the chip between triggers. Excess noise is observed at the output of the APSP. This has been traced to cross-talk between the read and write lines of adjacent channels of the pipeline memory and the layout of the next version of the chip has been suitably modified.

3. Optical link

The analogue optical read-out system being developed by the RD23 collaboration is shown schematically in fig. 8. It is based on a reflective link between a transceiver on the read-out end and an asymmetric Fabry Perot modulator (AFPM) on the front end. The concept satisfies requirements for radiation hardness, low power dissipation and small cabling bulk in the detector area while allowing an easy maintenance of sensitive components such as lasers and high density electronics in the crate racks. A brief description of the link functionality follows; a thorough discussion can be found in [7].

A 1.55 μm semiconductor laser injects continuous wave (CW) light into a standard telecom single mode fibre of 8 μm core diameter towards the front-end module. There, the AFPM converts the multiplexer sampled voltages into optical signals by varying its reflectance, thus both modulating the incoming light and sending it back to the receiver through the same fibre. At the transceiver end of the chain, a high gain, low noise transimpedance amplifier converts the detected signal to a voltage of sufficient amplitude to be digitised and processed.

Fig. 9 illustrates the 4 channel set-up used during the beam tests. On the front-end side, the monolithic modulator array (2) consists of 4 vertical cavities (InGaAs/InP) of ~30 μm diameter on a 250 μm pitch [14]. It is packaged in a prototype housing where diffused glass micro-lenses relay the light from the cleaved fibre tips to the modulators and vice versa. To avoid multi cavity effects, all air interfaces on the beam path are anti-reflection coated. From a system point of view, the electro-optic modulator can be considered as having electrical inputs and optical outputs. A buffer stage (1) interfaces between the multiplexer outputs and the AFPM electrical inputs. It performs amplitude matching, level shifting and protective functions. The pigtailed optical outputs are connected to the 70m long fibre ribbon using angle polished MT4 ferrules [15] in MPO4 shells with return losses greater than 50 dB.

On the read-out side, the distributed feedback laser (3) is biased at ~3 mW optical power. A high frequency (200 MHz) dithering signal is superimposed on the laser DC bias current to broaden its linewidth thus reducing the phase to intensity noise generated in the external cavity [16]. After the isolator, fused 1:4 splitter and 2×2 coupler (4), a power of about 200μW at the output of the MPO4 connector is launched towards the modulator. The modulated light signal reflected back onto the photodiode amounts to ~2μW peak to peak if the modulator is driven to the edge of its linear range (~3 V peak to peak). A high gain (600 kV/A), low noise (2.5 pA/√Hz), two stage transimpedance amplifier (5) converts the photocurrent into a voltage, with the bandwidth limited to 20 MHz. The peak signal to rms noise ratio of the link measured in the lab under these conditions was better than 100:1.

4. Experimental arrangement for the beam test

Figure 10 shows a schematic illustration of the system. The silicon microstrip detector (see section **4.1**) was positioned in the beam between fast scintillator counters which generated a trigger when a particle traversed the instrumented area of the detector. The detector was bonded to an APV3 read-out chip, the outputs of which were buffered and fed to sample-and-hold and multiplexer circuitry. The multiplexer outputs were transmitted to the control room via coaxial cables or by fibre. The apparatus was placed in the CERN X5 beam line, operating in a mode supplying a mixture of 100 GeV electrons and pions to obtain the maximum particle flux. Up to 100 events were gathered in each 2 second beam spill, depending on the beam quality.

Control electronics in the beam area were required to operate the sample-and-hold and multiplexer functions and for interfacing control signals from the control room to the front end circuitry. The data acquisition (DAQ) system was located in the control room. The multiplexer outputs were digitised by a flash analogue-to-digital converter (FADC). A time-to-digital converter (TDC) was used to record the arrival time of the beam particle (or calibration pulse) with respect to the 40 MHz system clock. A sequencer unit generated the digital signals required to operate the system and a further custom circuit (the Pipeline Location Triggered Register) allowed recording of the actual locations triggered in the pipeline. The DAQ system was controlled by a Macintosh running LabVIEW.

4.1 The detector

The detector used for this test was a single-sided microstrip device, with integrated ac-coupling and polysilicon biasing, produced at SINTEF, Oslo, Norway as part of a batch of RD20 [4] prototypes. The detector was 350 μm thick, reaching full depletion at ~60V, with 128 strips, 5 cm long and 12 μm wide on a pitch of 50 μm. During the beam test it was operated with 100V bias. Typical values for the polysilicon resistors were 2 MΩ, with a spread of ~30%. An additional layer of silicon nitride was used in the processing to improve the yield of the coupling capacitors, with no shorted capacitors found in more than 4500 tested. The nitride layer covered the entire surface of detector, which leads to increased surface currents [4], but these currents, typically ~10 nA/strip/cm at room temperature, are stable and do not contribute to the noise in the system due to the fast shaping. Measurements on test structures from the same wafers indicate that the total strip capacitance was about 1.3 pF/cm, measured at 1 MHz and 100V bias.

4.2 Control and data acquisition electronics

The operation of the sequencer which was located in the control room was central to the functioning of the complete system. The sequencer is a custom built VME module [17] which provided the digital signals required for the front end chip operation, multiplexing and analogue to digital conversion. It is essentially a programmable digital pulse generator which can generate up to 22 parallel pulse trains at user selectable rates up to 67 MHz. In this setup the sequencer was used to generate the 40 MHz clock, the reset and the level one trigger pulse (T1) required by the APV3 chip, as well as a 10 MHz multiplexer clock and the convert signals for the FADC. The 40 MHz clock ran continuously, while the APV3 reset, T1, multiplexer and FADC signals were only required in response to a beam (or calibrate) trigger from the front end. To facilitate this the sequencer was programmed to enter an idle loop, jumping to the read-out sequence following a trigger generated by a beam particle or a calibrate pulse. After read-out the module returned to the idle loop and waited for the next trigger.

The operation of the hardware can be illustrated by describing the sequence following a trigger generated by a particle. In calibrate mode, a free running oscillator was used to generate a trigger synchronised with the calibrate signal to the APV3 read-out chip. In the control room the trigger was passed to the sequencer and was also used to start a TDC (LeCroy model 2288A with ~50 ps. resolution). The 40 MHz sequencer clock was used to stop the TDC, hence the digitised value represented the arrival time of the trigger with respect to the APV3 pipeline sample time. This allowed optimally timed events (which occur in phase with the clock edge, as would be the case in a synchronous system such as LHC) to be selected in the off-line analysis using the TDC information.
The APSP circuit operates synchronously with a 1 MHz clock internally derived from the 40 MHz clock, hence the APSP may not actually commence operation until up to 1μs after receiving the T1. A 1 MHz strobe pulse from the chip is provided to allow external circuitry to synchronise with the APSP cycle. During APSP operation four voltage levels appear sequentially at the output (fig 6), simultaneously for all 32 parallel channels. The first three levels correspond to the three voltage samples from the pipeline, the fourth being the deconvolution result. Following a T1, external circuitry was used to count strobe pulses to determine when to sample the APSP outputs, so either the deconvolution result or any of the individual samples could be read-out. The voltage levels were then multiplexed onto four outputs for transmission to a 4-channel 8-bit FADC [Dr.B.Strück model DL401] via the optical link or coaxial cables. Of the 32 channels available on the APV3 chip only 28 were utilised since it was necessary to transmit a reference level (ground), so each multiplexer channel transmitted signals from 7 detector strips. Multiplexing was performed under sequencer control at 10 MHz, the fastest rate possible for the commercial multiplexer chips used.

The Pipeline Location Triggered Register (PLTR) recorded the locations within the APV3 pipeline from which the data originated. Eight bits of the sequencer output were programmed as a 40 MHz counter which incremented continuously from 0 through 159 during the idle loop (the pipeline has 160 locations), starting immediately after a Reset signal. Consequently the counter value at the PLTR input was synchronised with samples in the pipeline. Following a trigger the first operation was to save the value in the PLTR which was then stored with the data from the event using an additional data input facility provided by the sequencer module. The APV3 actually provides the current pipeline cell address but, for practical reasons, this output was not made use of in this test.

4.3 On-line software

A Macintosh IIfx running LabVIEW controlled the DAQ. The data acquisition rate was limited to approximately 25% of the scintillator trigger rate, partially because of the speed at which the software could address the hardware, but also because of the 30% deadtime introduced by the sequencer cycle. These gave the primary limit on the statistics. A CAMAC register was set by the computer to enable the hardware when the DAQ system was free. Data were written to the hard disk at the end of each beam spill.

4.4 Trigger generation and performance in the beam

Fig 11 shows a schematic illustration of the trigger system. Two scintillator counters detected the passage of a beam particle through the silicon detector. The upstream scintillator was 3 mm wide and was aligned to cover the 1.4 mm instrumented width of the silicon. The second scintillator was 10 mm wide and therefore only coarse alignment was required to ensure that a beam particle which traversed the narrow scintillator and the detector also traversed the wider scintillator. The outputs of both scintillator counters were discriminated and passed to a coincidence unit, one being delayed so that the trigger timing edge was derived only from the 10 mm scintillator. As the 3 mm scintillator was wider than the instrumented strips, only 47% of the beam triggers resulted in a detectable signal in the silicon. Because there were 28 instrumented strips the probability of a signal in a single strip (with no charge sharing between strips) was 1.7%. The main emphasis in this test was on aspects other than detector spatial resolution and no attempt was made to utilise a microstrip telescope to enhance this offline.

The trigger performance was investigated in the beam by using the discriminator outputs from the two scintillators to start and stop the TDC. The resulting TDC spectrum is shown in fig 12 and approximates to a gaussian distribution, with a tail below the peak attributed to larger pulses which cause one of the scintillators to fire early. The distribution is believed to be asymmetric because the thresholds were not identical. The standard deviation of the central peak of the distribution was 250 ps, hence the trigger jitter due to only one scintillator was 177 ps, which was more than sufficient for system timing requirements.

The deconvolution filter employed by the APSP has a weighting function which results in zero output for triggers which arrive either early or late by more than one clock cycle (see figure 7). This is a narrow window, and therefore, to maximise data taking efficiency, it was important that propagation delays in the trigger logic were well enough known that the T1 signal to the APV3 arrived with a precise delay following a trigger generated by a beam particle. It was found easiest to guarantee this by calibrating the system with a slightly modified trigger.

In calibrate mode, beam pulses in the 10 mm scintillator were used to generate the calibrate signal to the APV3 and the trigger coincidence unit was configured to fire irrespective of the state of the 3 mm scintillator. In this way the calibrate pulses arrived late at the APV3 input, compared to a genuine beam particle signal, but there was a simple relation to the normal beam trigger, as the only unmeasurable delay was the transmission time of signals in the photomultiplier. This enabled the correct timing of the T1 signals to be established quickly on-line.

4.5 Optical link performance in the beam

The overall optical link performance was evaluated by comparing its response to a coaxial transmission line of 20m length, transmitting identical signals. The

transimpedance amplifier outputs were measured with an 8 bit digital oscilloscope at 100 MHz sampling rate. The measured waveforms from the two transmission media were normalised and the relative delay was determined by cross-correlation. Since the multiplexer ran at 10 MHz, each level from a single detector channel was sampled ten times by the oscilloscope and one of the ten values was selected for comparison with the corresponding sample transmitted via the optical link. Fig. 13 shows the statistical distribution (over 160 events) of difference between the two signals, measured simultaneously with both links. Taking the coaxial transmission line as a reference, the optical link noise and distortion was 8.4 mV rms, to be compared to 170 mV signal amplitude corresponding to a 2 MIP (Minimum Ionising Particle) most probable energy loss (0.8 V at the modulator input). It should be noted that this represents not only noise associated with the optical link but also a contribution due to the small non-linearity of the transfer characteristic. The link noise measured in the laboratory was 5.5mVrms, measured on a periodic pulse sequence. Because of baseline fluctuations at the APV3 output in the beam test, only 25% of the available linear range was used. As a consequence the data in fig. 13 contain an extra error contribution due to distortion of 2MIP signals which does not actually contribute significantly to the final signal to noise ratio.

The optical link was operated continuously for 36 hours with no degradation of the signal or noise characteristics. The only adjustments needed were due to the effects of temperature fluctuations in the beam area (a drop of 3°C overnight) (section 5.1.2). Such variations in the packaged device used in this test cause the micro-optical elements, which focused the light from the fibre into the modulator cavity to drift out of alignment and induce a modification of the AFPM insertion loss[1]. In consequence of the changing DC light level reflected back on the detector, the output offset voltage of the DC-coupled transimpedance amplifier tended to drift and even eventually saturate. During operation in the beam area, this effect made preventive adjustments of the offset settings necessary once every night. A baseline subtraction correction was implemented offline by monitoring a grounded multiplexer channel.

5. Data analysis

The primary objective of this beam test was to demonstrate the operation of the complete read-out chain in a beam environment since both the front end electronics chip and the optical link are quite novel technological developments. However it was essential to evaluate the performance quantitatively to gain some insight into the further improvements required for LHC operation and to compare the operation of the electrical transmission line with optical data transmission. Without a beam telescope it was not possible to select data only from strips which should have recorded particle hits, therefore in the pulse height distributions noise entries greatly outnumber particle signals. From the geometry of the system the fraction of events above the noise is expected to be 1.7%, compared with the value of 1.2% which is measured in the data. This is sufficiently low that statistically valid noise calculations can be performed using data taken whilst the beam was operational without making cuts to find non-hit channels.

[1]Although adequate for lab evaluation, this package is not temperature stable. A better housing has since been fabricated, where the fibres are directly butt coupled to the modulator substrate.

5.1 Data processing

During the test it was evident that common mode noise was present, which can be reduced by averaging the baseline data across all channels. Several contributions to the common mode noise were identified: variations in the baseline level of each event associated with the pipeline cell used to store the data, variations due to the optical link and baseline level fluctuations in the system which were common to all channels (excluding those above). The analysis was divided in this way to improve the understanding of the noise contributions in the system. The sequence of operations has no effect on the final result, but was chosen for ease of processing. Separation of effects due to pipeline cell pedestal variations improves over a simple common mode noise calculation by removing effects due to possible differences in value between pipeline cell capacitors.

5.1.1 Pipeline cell variations

The mean level of an output sample from the APV3 pipeline is found to vary from cell to cell, giving rise to a series of pedestals associated with each of the 32 individual pipelines. For each trigger the PLTR records a single value which identifies the locations in the pipeline read out by the APSP (as described earlier), thus the mean value of the pedestal associated with each PLTR value can be calculated. Since the APSP uses 3 pipeline samples for deconvolution, the deconvoluted pedestal is a combination of values from 3 adjacent pipeline cells.

Fig 14 shows the results of the pedestal calculation for the 7 strips read by one multiplexer channel. It can be seen that the baseline level has a similar structure for all detector strips which indicates that some variations are common to each column in the array. The large pedestal fluctuations every 40 cells are almost certainly due to the 1 MHz APSP clock, as the effect is observed in 3 pipeline cell locations and in the ratio of the APSP weights. The fluctuation in the pedestals is positive in the first cell of the series, negative in the second, and slightly positive in the third, which is expected if spurious charge is injected into the pipeline at a single location since deconvolution operates on three cells.

5.1.2 Variation of optical link baseline offset

It was noticed during the test that the baseline level at the output of the optical link system changed gradually; fig 15 (a) shows how the baseline level changed with time. The gross trend was due to external temperature changes causing physical movements in the optical modulator assembly as described earlier in section 4.5. Much smaller oscillations, as shown in fig 15 (b), were also observed in the baseline level on a shorter time scale which are possibly associated with temperature stabilisation of other optical elements. All the fluctuations were eliminated by baseline subtraction; fig 19 (b), where the data were taken over several days shows this clearly.

5.1.3 Common mode noise

The remaining common mode noise can be calculated for each event by averaging the baseline value of all channels, excluding those containing signal. This average is then subtracted from the data for that event.

Fig 16 demonstrates the presence of common mode noise in the system. The signal observed in one channel is plotted against the signal observed in another (non adjacent) channel. Fig 16 (a) clearly shows a correlation between channels in the system and figs 16 (b) and (c) show that noise is reduced after subtraction of the pipeline pedestal variations and the optical link baseline level fluctuations. The last plot, fig 16 (d), shows the data after all common mode subtractions.

5.2 Signal extraction

Fig 17 shows the improvement in signal as the corrections applied above are made to the data. Figure 18 (a) shows the signal normalised to the rms noise level for all strips read through one multiplexer channel (7 strips), and optical fibre. Fig 18 (b) shows an equivalent histogram of the signal to noise for all strips summed for data transmitted using coaxial cable. It is possible to combine data from all 28 strips in this case because the attenuation of each multiplexer channel was set to be identical.

These are not yet the final results as the data were gathered asynchronously, and therefore contain events out of phase with the clock cycle. Signals from these events are consequently reduced in magnitude by the deconvolution filter, and therefore smear the pulse height distribution from the Landau form.

5.3 The effect of the weighting function

The time delay between a trigger signal and the following clock pulse is measured by a TDC as described in section 4.2. The temporal transfer function of the APSP (discussed in section 2.1) is known as the weighting function. Its form as measured in the laboratory is shown in fig 7. Fig 19 (a) shows the weighting function measured in the test beam using an asynchronous test pulse applied to the inputs of the APV3 chip. Figure 19 (b) shows the pulse height of beam triggered events against TDC value. It shows a large band of hits at zero pulse height, which represent noise, and signals for events generated by beam particles distributed above this in the form of the weighting function. By selecting events which occur in an appropriate time interval (in fig. 19 (b) approximately TDC channels 500 to 600), an approximation to a synchronous system can be obtained.

5.4 Signal to noise of synchronous events

Histograms of the normalised pulse height distribution after making a 5 ns wide TDC cut to the data, and processing it as above are shown in fig 20. The histograms were compiled using all available data from all strips in both cases. The most probable signal to noise of the data using optical transmission is found to be 11.5:1 and, using electrical transmission, it is found to be 10.5:1. The difference between the two values is thought to be statistical. A minimum ionising pion of 100 GeV/c is calculated to have a most probable energy loss of 110 keV in a silicon layer of thickness 350 μm [18,19]. A landau distribution has been convoluted with a gaussian of standard deviation corresponding to a noise of 2700e^- and superimposed on the histograms. Reasonable agreement is seen between the form of the landau distribution and that of the histograms, although the excess signal at lower levels is attributed to charge sharing between strips.

The APV3 amplifier with this detector load is expected to have a noise of 1500e^-, which is smaller than our measured value. This is believed to be due to cross talk from

the pipeline read and write lines (section 2.2). We expect a substantial improvement in future versions of the chip. Although the noise associated with the pipeline prevents realisation of the full performance of the system, considering the complexity of the design these faults are minor inconveniences at this stage of prototyping .

6. Conclusions

A prototype of an LHC tracking detector read-out system using radiation hard analogue front end electronics and an electro-optic modulator device for data transfer over an optical fibre link has been demonstrated for the first time in a test beam. The performance is close to that required for operation at LHC and improvements already incorporated in further versions of the components now in production are expected to bring it still closer to the specifications for the CMS experiment in the near future.

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References

[1] CMS Technical Proposal. CERN/LHCC 94-38 (December 1994)
[2] Atlas Technical Proposal. CERN/LHCC 94-43 (December 1994)
[3] G. Hall, *Front end electronics for silicon tracking at LHC.* IEEE Trans in Nucl. Sci. 41 (1994) 1086-1090.
[4] RD20 Status Report 1992. CERN/DRDC 92-28 (May 1992)
RD20 Status Report 1993. CERN/DRDC 93-30 (August 1993)
RD20 Status Report 1994. CERN/DRDC 94-39 (October 1994)
[5] Harris Corporation, Semiconductor sector, P.O. Box 883, Melbourne, Florida, U.S.A.
[6] M. Raymond, G. Hall, M. Millmore, R. Sachdeva, M. French, E. Nygård, K. Yoshioka, *Measurements of transistors and silicon microstrip detector read-out circuits in the Harris AVLSIRA rad-hard CMOS process.* Nucl. Instr. & Meths. A 351 (1994) 449-459.
[7] RD23 status report. CERN/DRDC 94-38 (1994)
[8] A. Baird, J. Dowell, P. Duthie, K. Gill, M. Glick, N. Green, G. Hall, R. Halsall, G. Jarlskog, I. Kenyon, A. Moseley, S. Quinton, G. Stefanini, N. Try, F. Vasey, K. Webster, *Analogue lightwave links for detector front ends at the LHC* IEEE NS Symposium, November 1994. To appear in IEEE Trans in Nucl. Sci.
[9] Marconi Defence Systems, GEC-Marconi Ltd, Stanmore, UK.
[10] G. Hall and G. Stefanini, *CMS tracker read-out system.* CMS/TN 94-137 (Jan. 1994).
[11] L.L. Jones, M. French, P. Seller and the RD20 Collaboration, *APV5-RH — A 128 Channel Analogue Pipeline for LHC.* To appear in IEEE Trans in Nucl. Sci. November 1994.
[12] S. Gadomski, G. Hall, T. Høgh, P. Jalocha, E. Nygard and P. Weilhammer, *The deconvolution method of fast pulse shaping at hadron colliders.* Nuclear Instruments & Methods in Physics Research A320 (1992) 217-227.
[13] Bingefors et al., *A Novel technique for fast pulse shaping using a slow amplifier at LHC.* Nucl. Instr. & Meths. A326 (1993) 112-119.
[14] C. Kirkby, M. Goodwin, A. Moseley et al., *Low voltage InGaAs/InP multiple quantum well reflective Fabry-Perot modulators for optical communications at microwave frequencies.* IEEE Proceedings-J, Vol. 139, No4, pp 249-53, 1992.
[15] S. Nagasawa, Y. Yokoyama, F. Ahiya and T. Satake, *A High-Performance Single-Mode Multifiber Connector Using Oblique and Direct Endface Contact Between Multiple Fibres Arranged in a Plastic Ferrule.* IEEE Photonics Technol. Lett., Vol. 3, No10, pp937-9, 1991.
[16]. P. K. Pepeljugoski, K.Y. Lau, *Interferometric Noise Reduction in Fibre-Optic Links by Superposition of High Frequency Modulation*, J. of Lightwave Technol., vol 10, No. 7, pp957-63, 1992.
[17] The sequencer was designed at the Rutherford Appleton Laboratory by M. Morrisey.
[18] G. Hall, *Ionisation Energy Loss Of Highly Relativistic Charged Particles In Thin Silicon Layers.* Nucl. Instr. & Meths. 220 (1984) 356-362.
[19] R.M. Sternheimer, S.M. Seltzer, M.J. Berger, *The Density Effect For The Ionization Loss Of Charged Particles In Various Substances* . Atomic & Nucl. Data Tables 30:261,1984

Captions

Fig 1. Schematic of the APV3 amplifier.
Fig 2. Typical APV3 amplifier pulse shape, and the voltage samples stored in the pipeline. One clock cycle is 25 ns.
Fig 3. Block diagram of the pipeline control logic.
Fig 4. Schematic of the switched capacitor implementation of the deconvolution filter.
Fig 5. Response of the APV3 amplifier to a test pulse equivalent to a minimum ionising particle, as a function of detector capacitance.
Fig 6. Two typical output sequences from the APV3, the second example shows a trigger following the injection of a test pulse.
Fig 7. The measured weighting function of the APV3.
Fig 8. Schematic of the optical link. The reflective MQW modulator is constructed as an asymmetric Fabry-Perot device (AFPM). A single optical fibre supplies laser light and carries the reflected pulse.
Fig 9. The arrangement of the principal elements of the optical link used in the beam test. The fibre ribbon was 70m in length.
Fig 10. Schematic diagram of the electronics, optical link and data acquisition and control system.
Fig 11. Hardware used to define trigger.
Fig 12. TDC spectrum using one trigger scintillator to start and the second scintillator to stop the TDC.
Fig 13. Statistical distribution of optical link noise as measured during beam tests.
Fig 14. Pipeline cell baseline variations for a series of strips.
Fig 15. Variations of optical link background level with time; (a) over several days. (b) over one hour, showing oscillations on a small time scale.
Fig 16. Channel 4 ADC count vs Channel 6 ADC count at various stages in the data processing; (a) Raw data. (b) Raw data after pipeline cell baseline fluctuations subtraction. (c) Further subtraction of optical link baseline fluctuations. (d) Further subtraction of common mode noise.
Fig 17 (a) Unprocessed data. (b) Data after subtraction of pipeline cell baseline fluctuations. (c) Data after subtraction of pipeline cell baseline fluctuations and optical link baseline fluctuations. (d) Data after subtraction of pipeline cell baseline fluctuations, optical link baseline fluctuations and common mode noise.
Fig 18. Signal to noise before a TDC cut; (a) with optical transmission (b) with electrical transmission. The graphs are not identical in form since both are from different time intervals within the weighting function cycle.
Fig 19 (a). Measured pulse height relative to clock edge after injection of a 2 MIP test pulse. The data come from more than one run since the maximum range of the TDC data in a single run corresponds to a single clock cycle (25 ns.). These data were obtained with a reduced multiplexer gain to accommodate this large test pulse signal. (b) Pulse height in ADC channels vs trigger delay in TDC counts. One TDC count corresponds to ≈50 ps.
Fig 20. (a) Signal to noise after a 5 ns TDC cut; (a) with optical transmission (b) with electrical transmission. Curve shows a landau distribution as explained in the text.

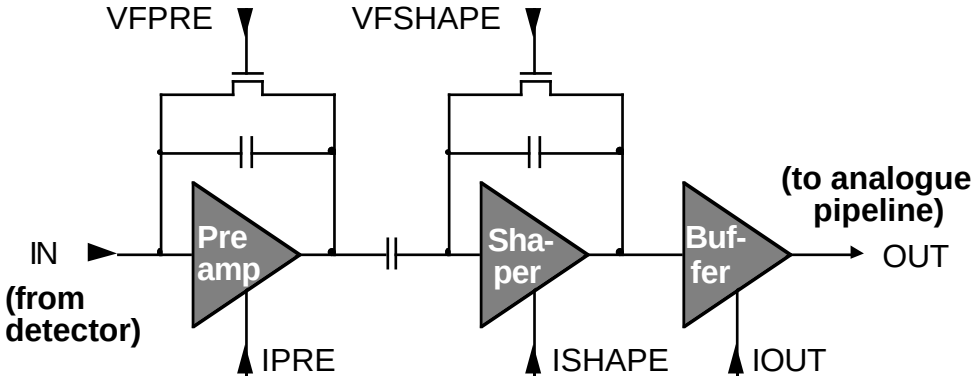

VFPRE
VFSHAPE
(to analogue pipeline)
IN
(from detector)
Pre amp
Sha- per
Buf- fer
OUT
IPRE
ISHAPE
IOUT

Figure 1

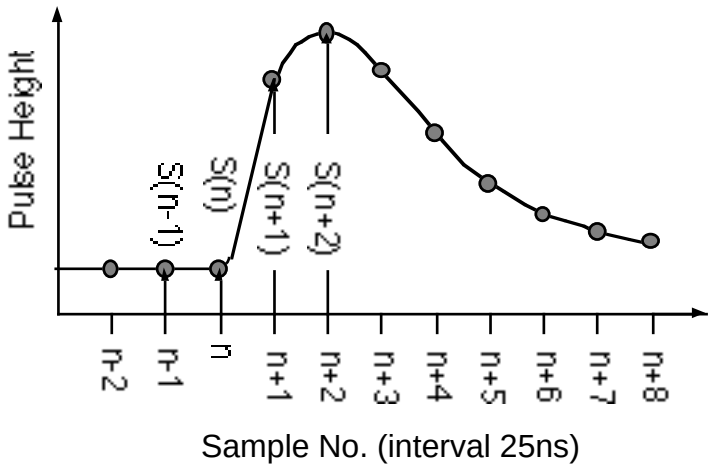

Pulse Height
S(n-1)
S(n)
S(n+1)
S(n+2)
n-2
n-1
n
n+1
n+2
n+3
n+4
n+5
n+6
n+7
n+8
Sample No. (interval 25ns)

Figure 2

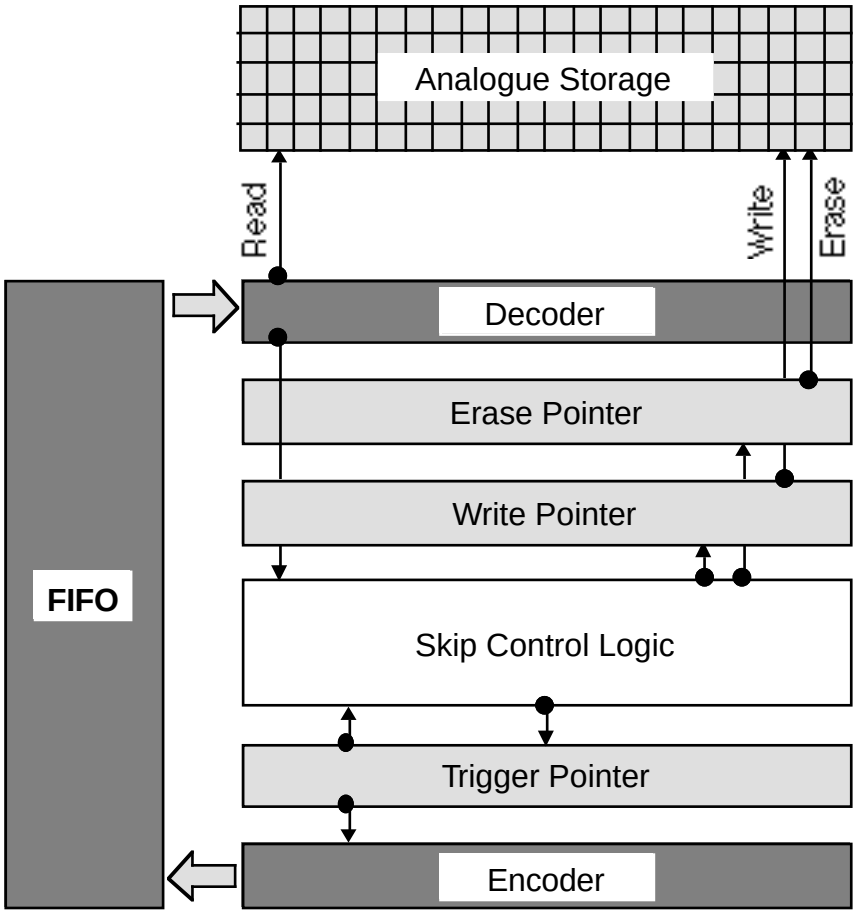

Analogue Storage
Read
Write
Erase
Decoder
Erase Pointer
Write Pointer
FIFO
Skip Control Logic
Trigger Pointer
Encoder

Figure 3

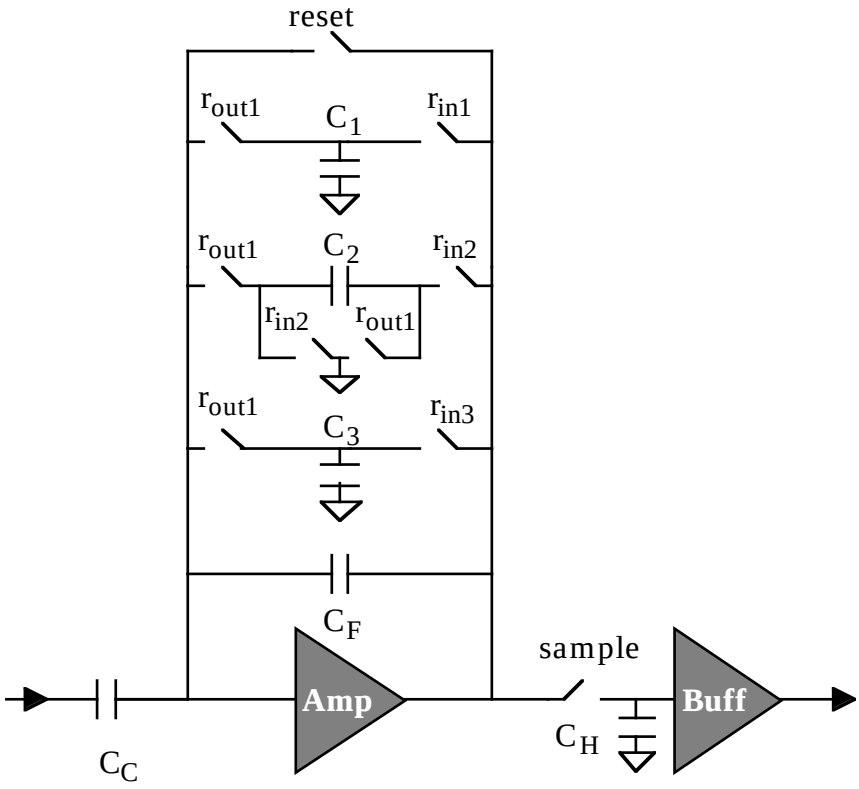

reset
r_{out1}
C_1
r_{in1}
r_{out1}
C_2
r_{in2}
r_{in2}
r_{out1}
r_{out1}
C_3
r_{in3}
C_F
sample
Amp
Buff
C_C
C_H

Figure 4

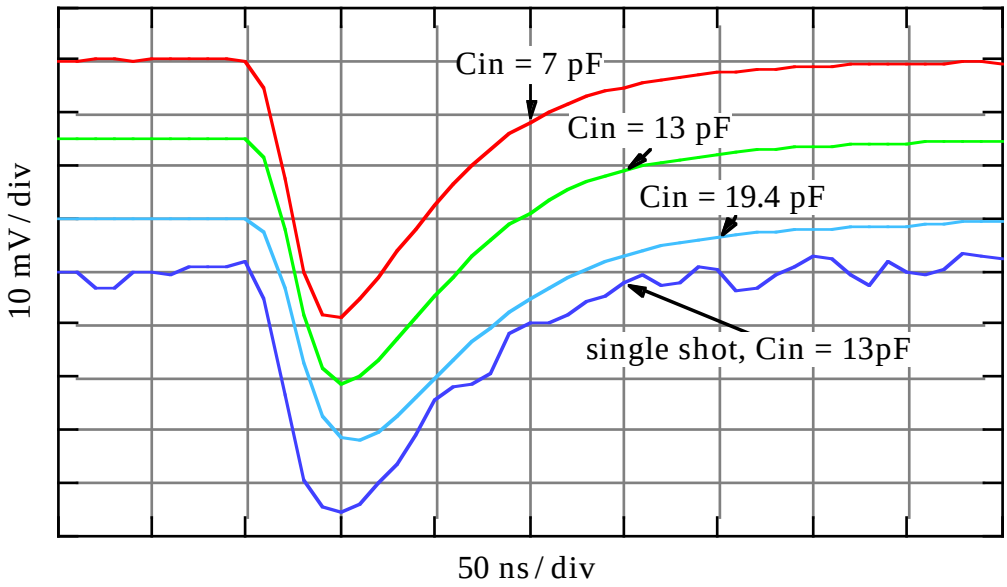

Cin = 7 pF
Cin = 13 pF
Cin = 19.4 pF
single shot, Cin = 13pF
10 mV / div
50 ns / div

Figure 5

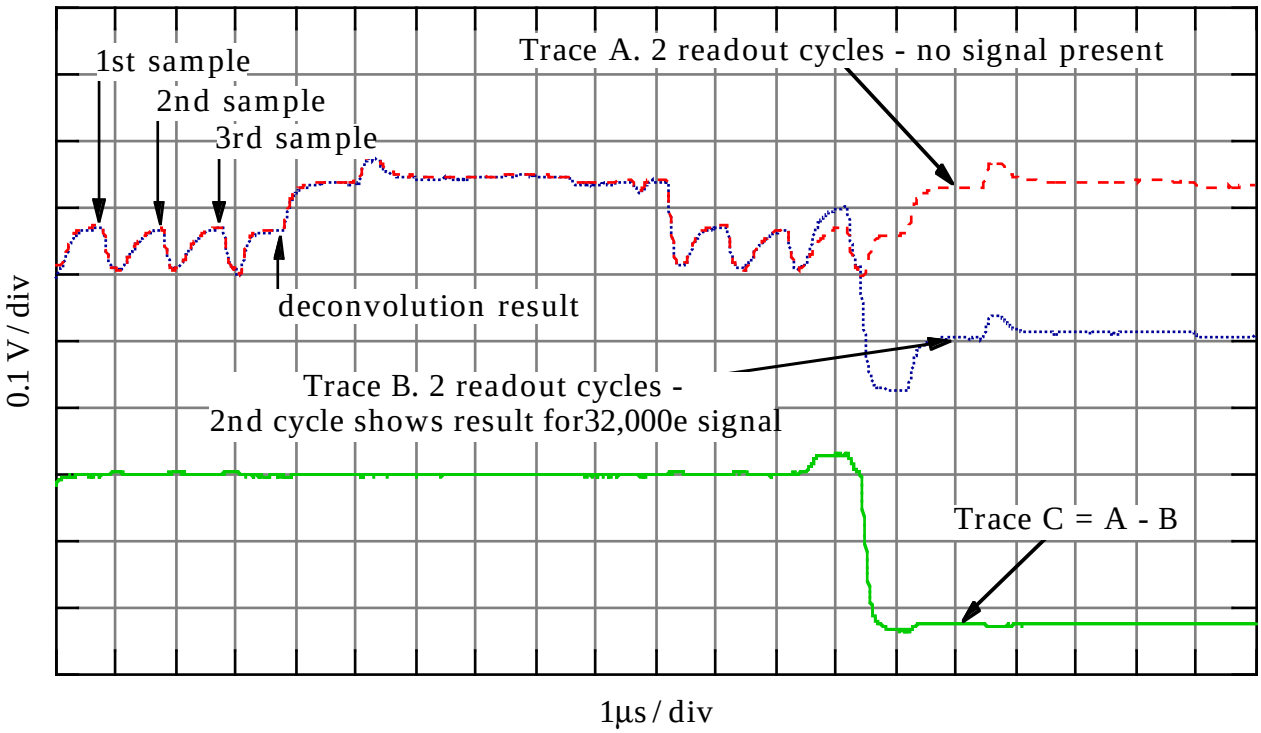

1st sample
2nd sample
3rd sample
Trace A. 2 readout cycles - no signal present
deconvolution result
Trace B. 2 readout cycles -
2nd cycle shows result for32,000e signal
Trace C = A - B
0.1 V / div
1µs / div

Figure 6

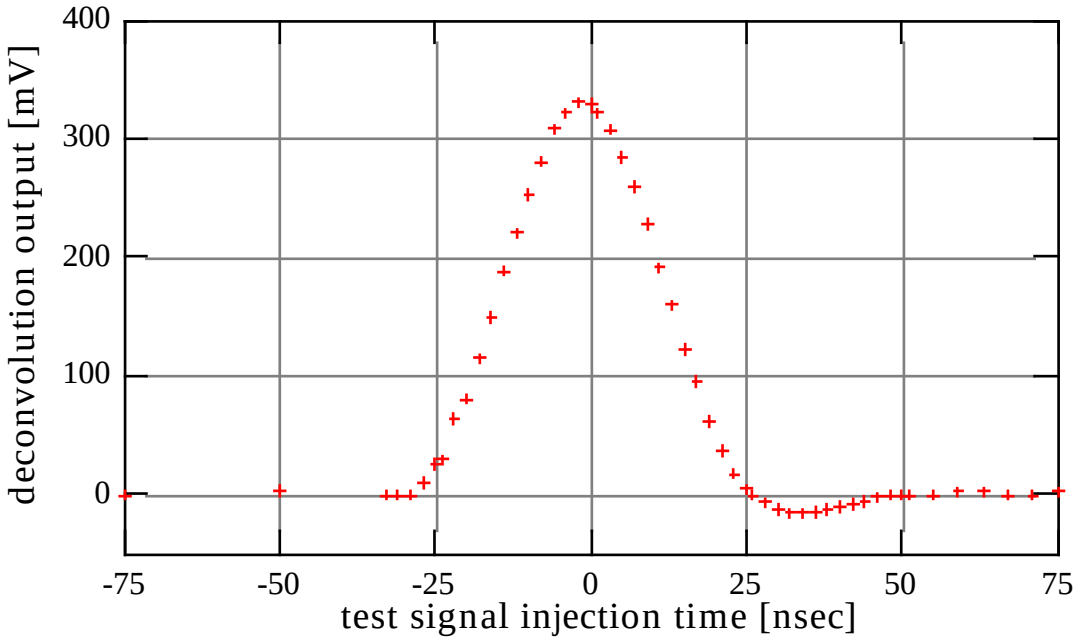

400
300
200
100
0
deconvolution output [mV]
-75
-50
-25
0
25
50
75
test signal injection time [nsec]

Figure 7

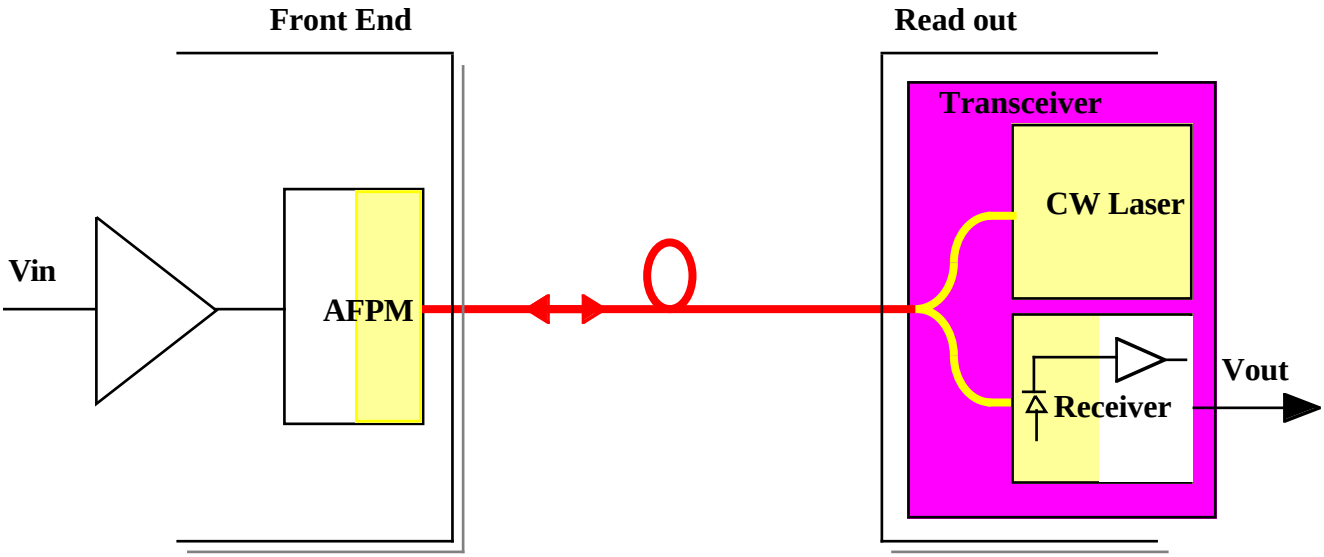

Front End
Read out
Transceiver
CW Laser
Vin
AFPM
Receiver
Vout

Figure 8

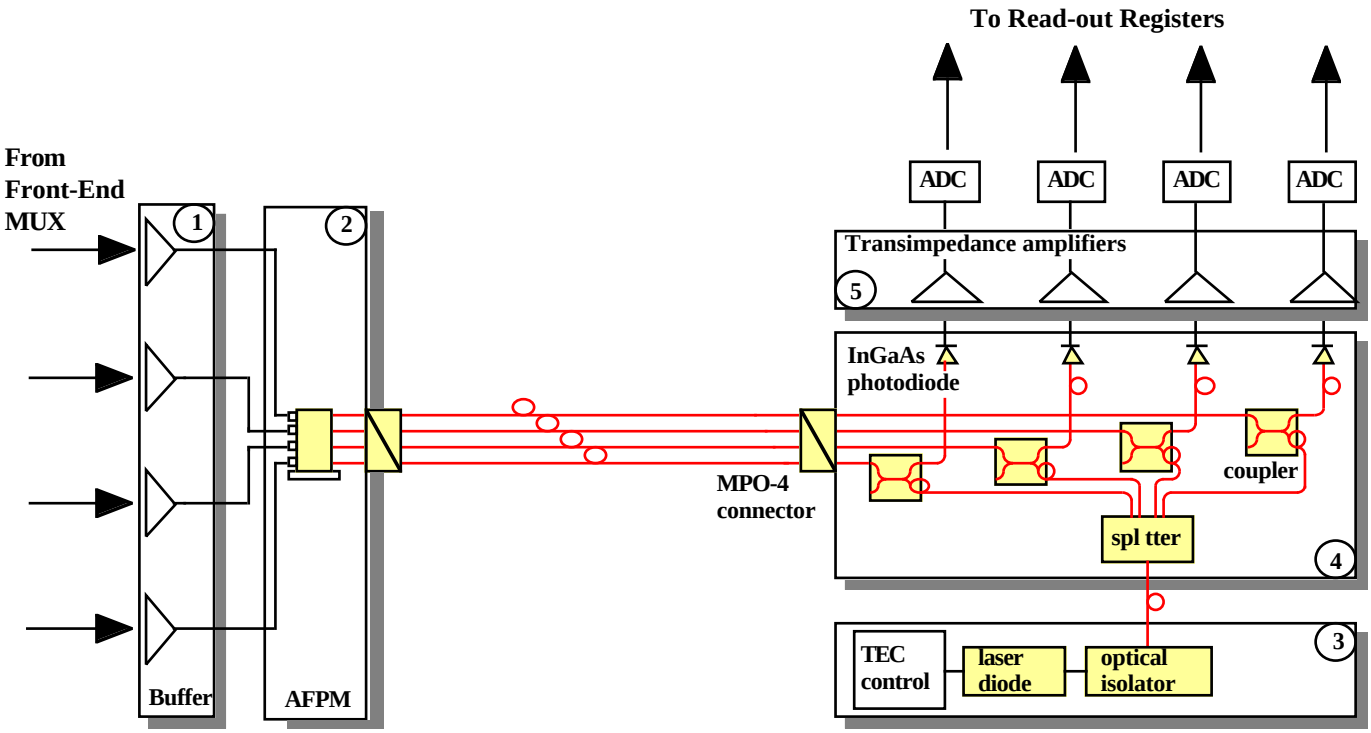

To Read-out Registers
From
Front-End
MUX
1
2
ADC
ADC
ADC
ADC
Transimpedance amplifiers
5
InGaAs
photodiode
MPO-4
connector
coupler
spl tter
4
TEC
control
laser
diode
optical
isolator
3
Buffer
AFPM

Figure 9

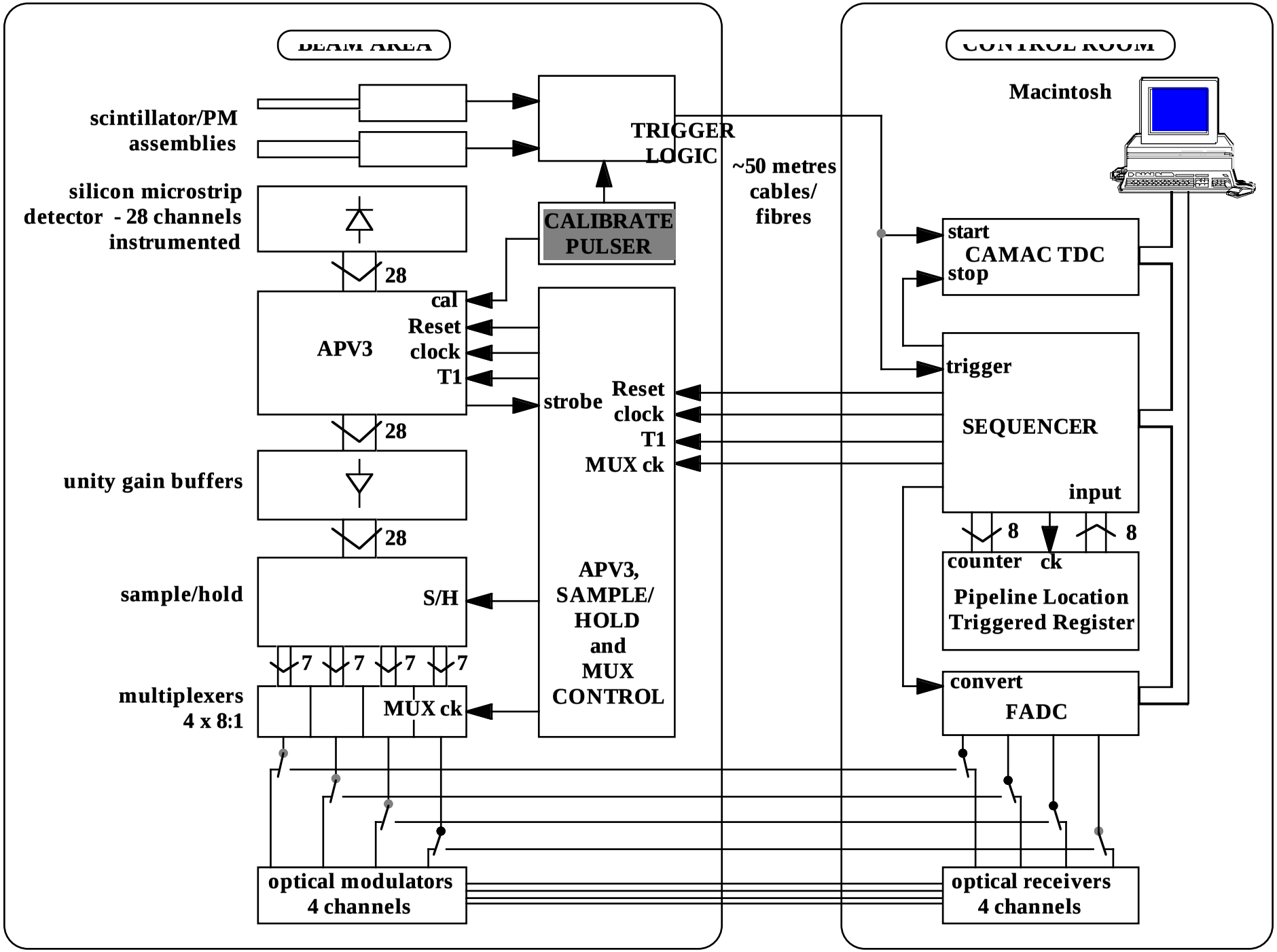

BEAM AREA
CONTROL ROOM
scintillator/PM assemblies
silicon microstrip detector - 28 channels instrumented
unity gain buffers
sample/hold
multiplexers 4 x 8:1
TRIGGER LOGIC
CALIBRATE PULSER
~50 metres cables/ fibres
Macintosh
28
cal
Reset
clock
T1
APV3
strobe
Reset
clock
T1
MUX ck
APV3, SAMPLE/ HOLD and MUX CONTROL
S/H
7
MUX ck
start
CAMAC TDC
stop
trigger
SEQUENCER
input
8
counter
ck
Pipeline Location Triggered Register
convert
FADC
optical modulators 4 channels
optical receivers 4 channels

Figure 10

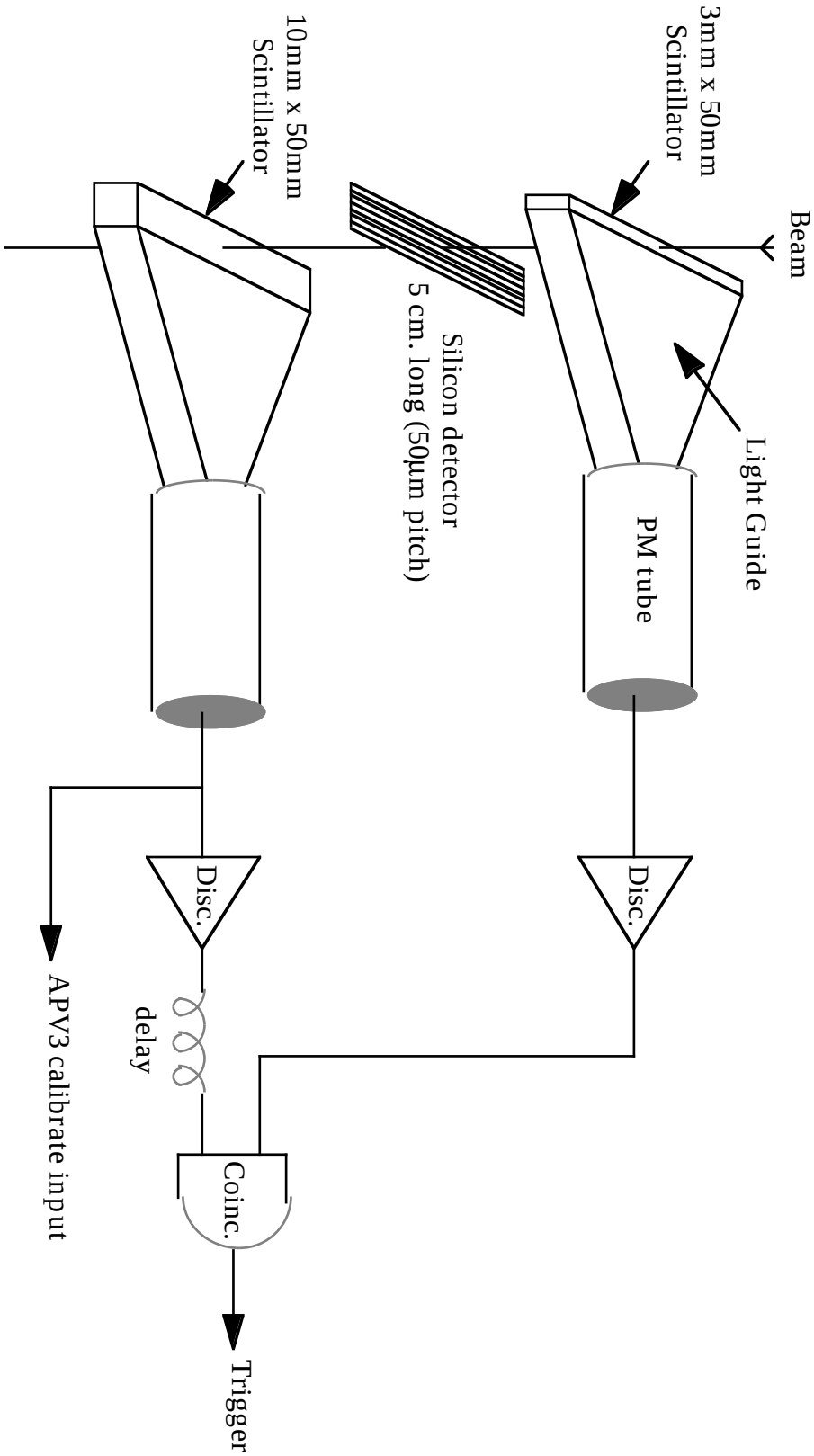

3mm x 50mm
Scintillator
Beam
10mm x 50mm
Scintillator
Silicon detector
5 cm. long (50μm pitch)
Light Guide
PM tube
Disc.
Disc.
APV3 calibrate input
delay
Coinc.
Trigger

Figure 11

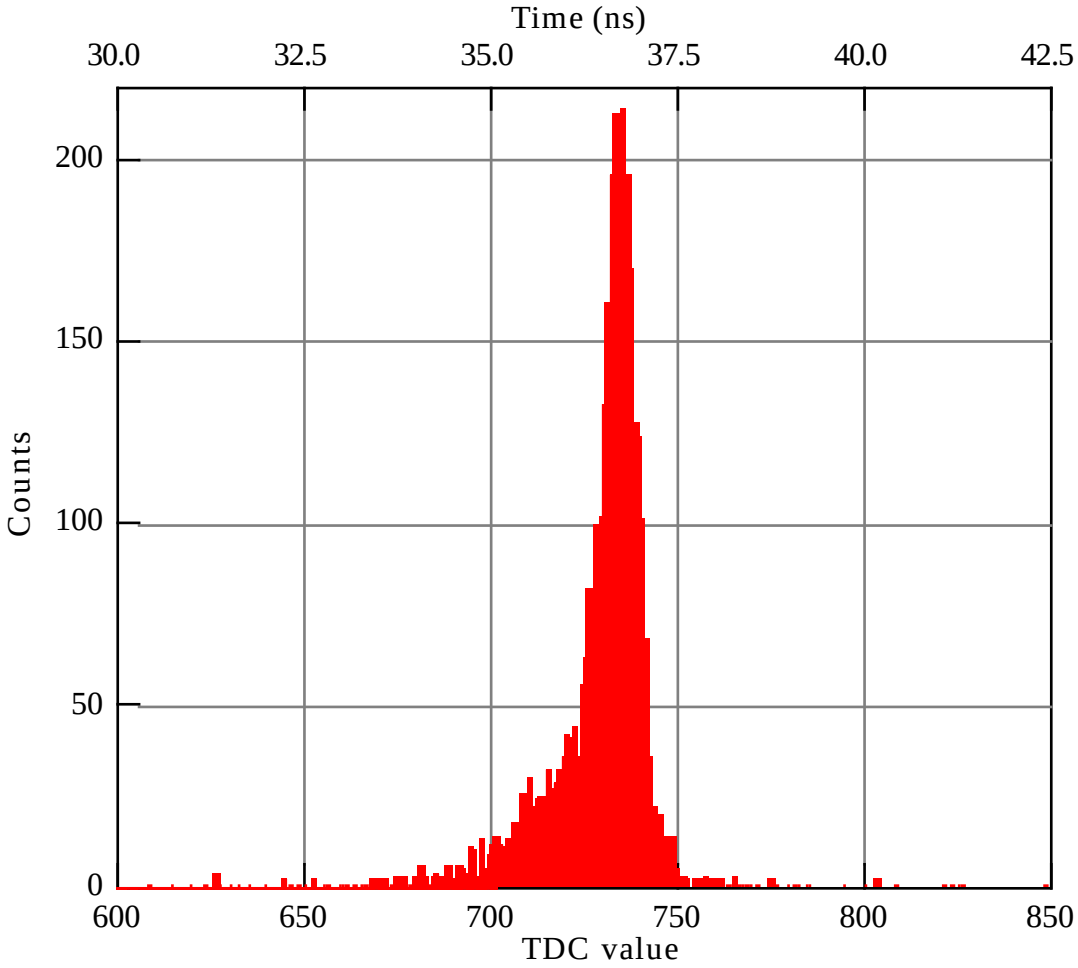

Time (ns)
30.0
32.5
35.0
37.5
40.0
42.5
200
150
100
50
0
Counts
600
650
700
750
800
850
TDC value

Figure 12

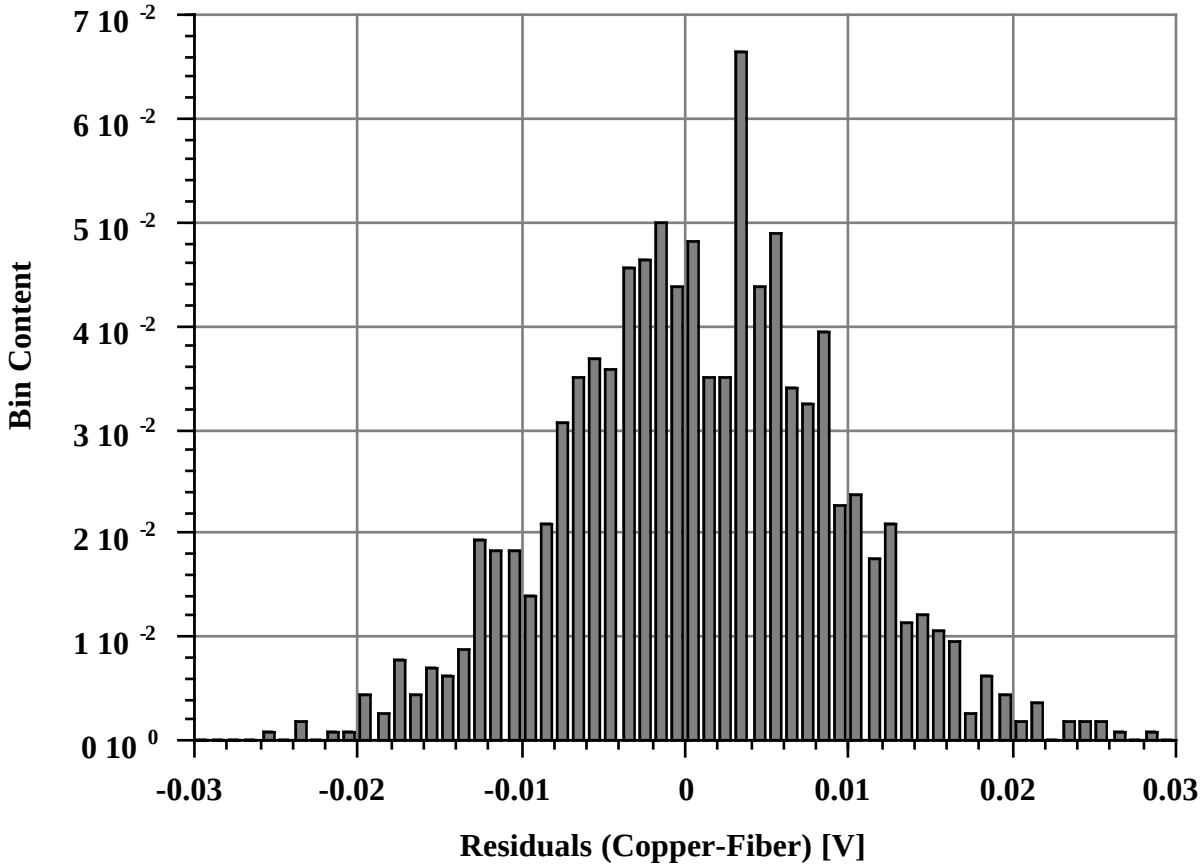

Bin Content
7 10 -2
6 10 -2
5 10 -2
4 10 -2
3 10 -2
2 10 -2
1 10 -2
0 10 0
-0.03
-0.02
-0.01
0
0.01
0.02
0.03
Residuals (Copper-Fiber) [V]

Figure 13

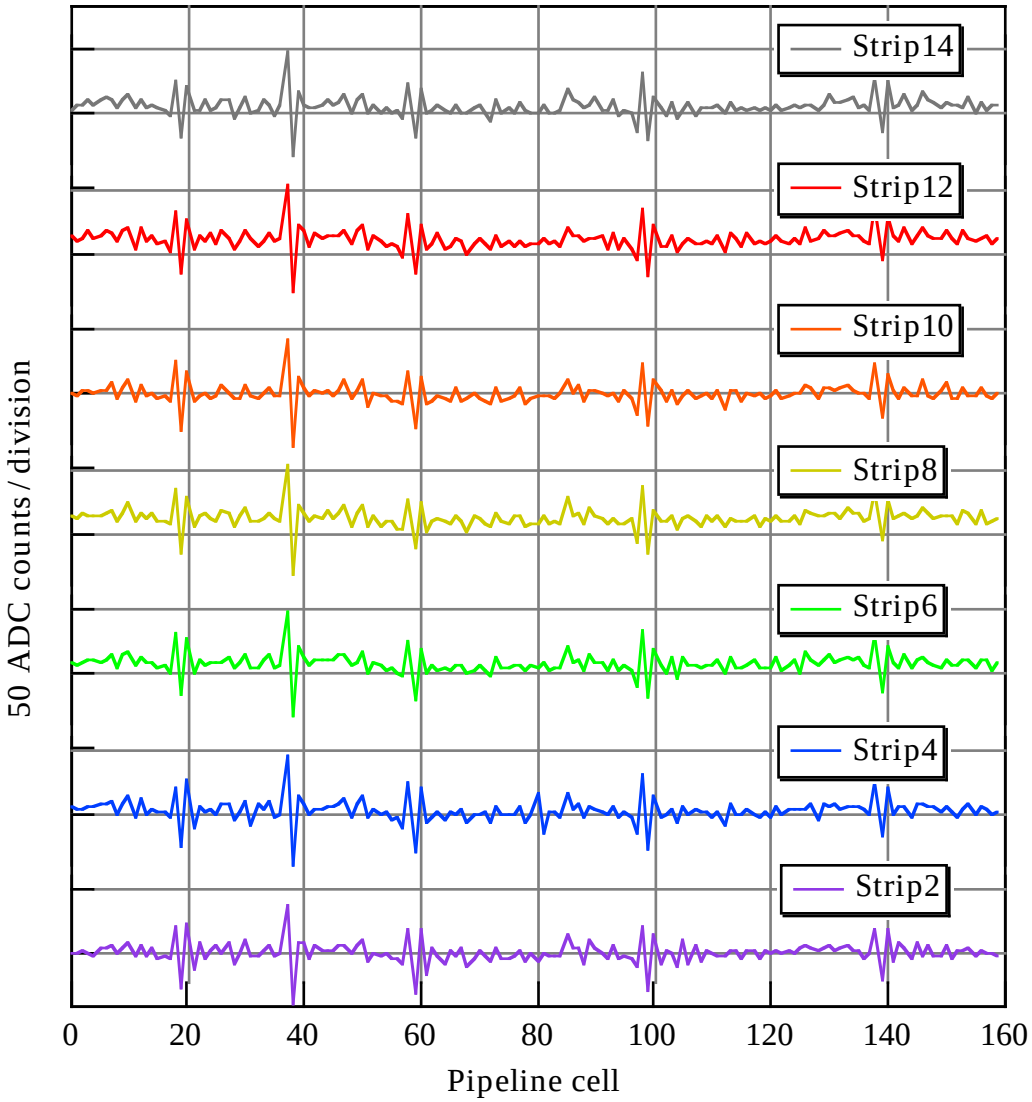
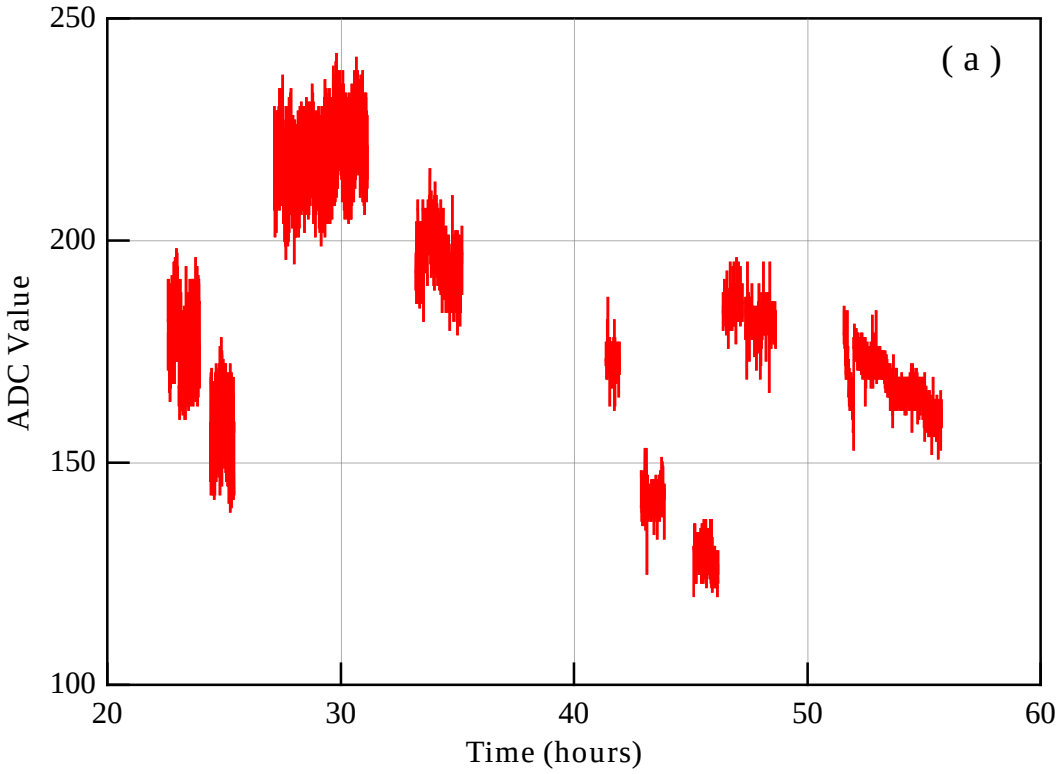
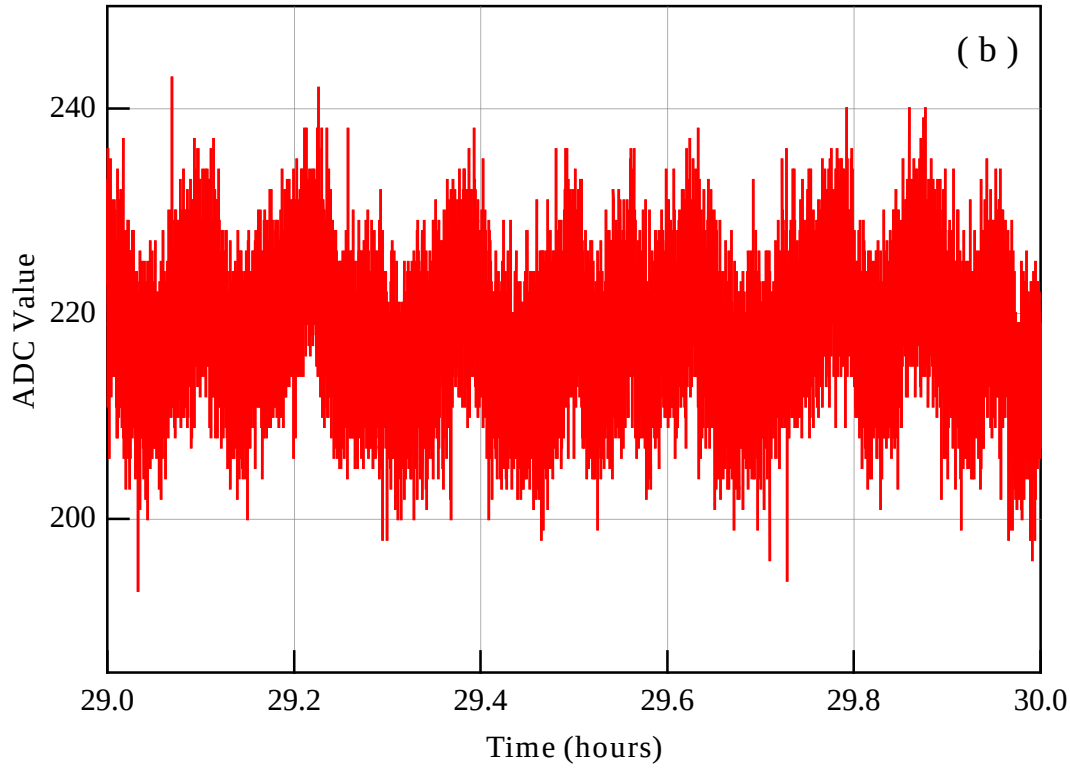

Strip14
Strip12
Strip10
Strip8
Strip6
Strip4
Strip2
50 ADC counts / division
0
20
40
60
80
100
120
140
160
Pipeline cell

Figure 14


(a)
ADC Value
250
200
150
100
20
30
40
50
60
Time (hours)


(b)
ADC Value
240
220
200
29.0
29.2
29.4
29.6
29.8
30.0
Time (hours)

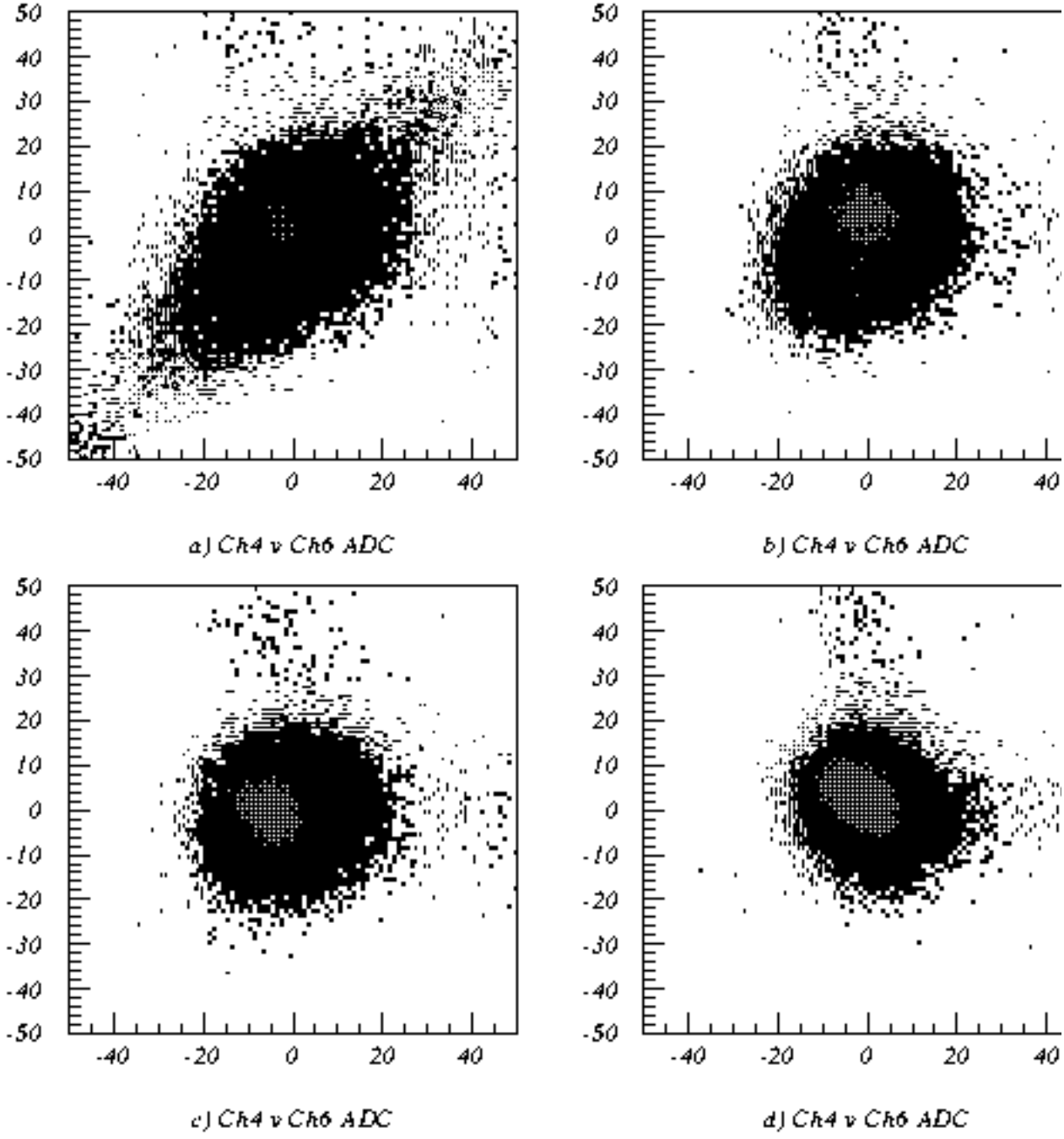


Figure 16

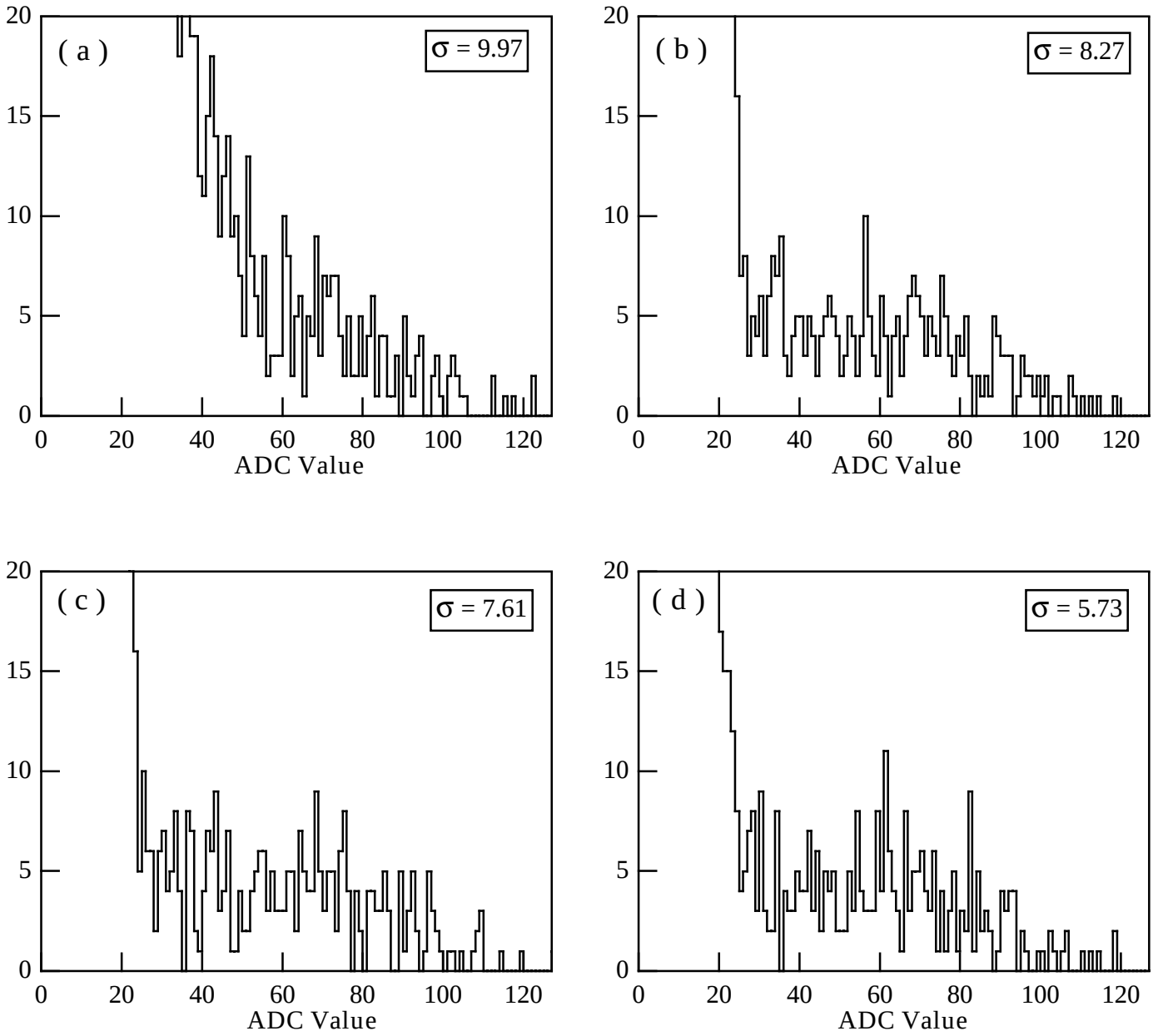
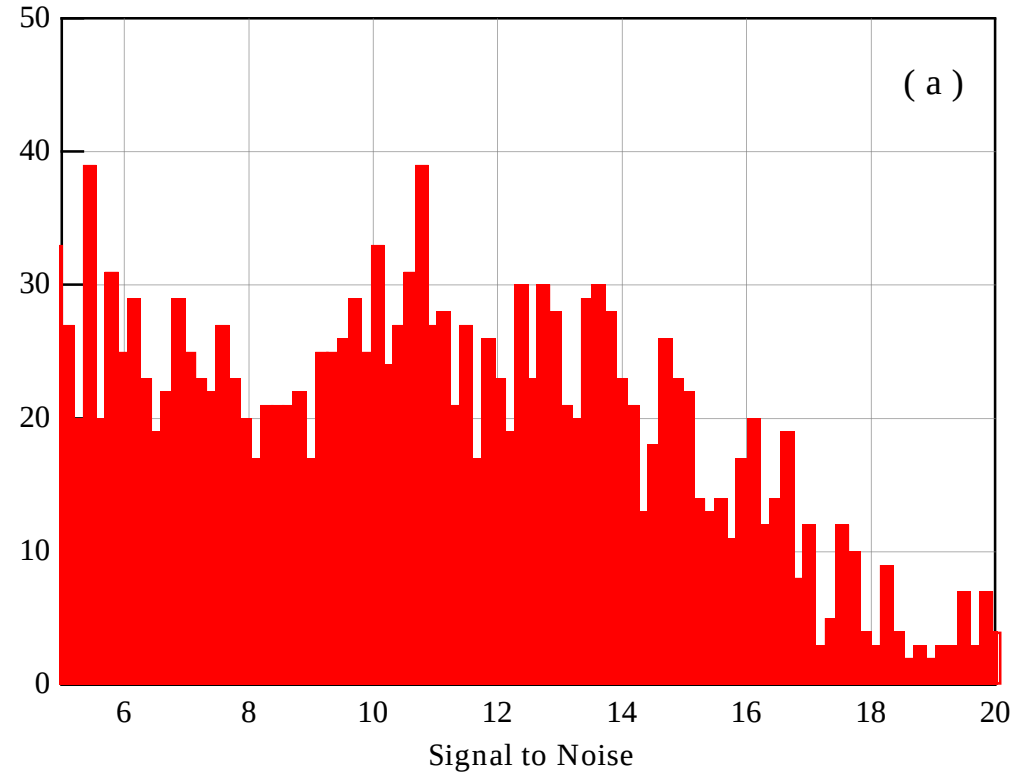

(a)
σ = 9.97
(b)
σ = 8.27
(c)
σ = 7.61
(d)
σ = 5.73
ADC Value
0
5
10
15
20
0
20
40
60
80
100
120

Figure 17


(a)
50
40
30
20
10
0
6
8
10
12
14
16
18
20
Signal to Noise

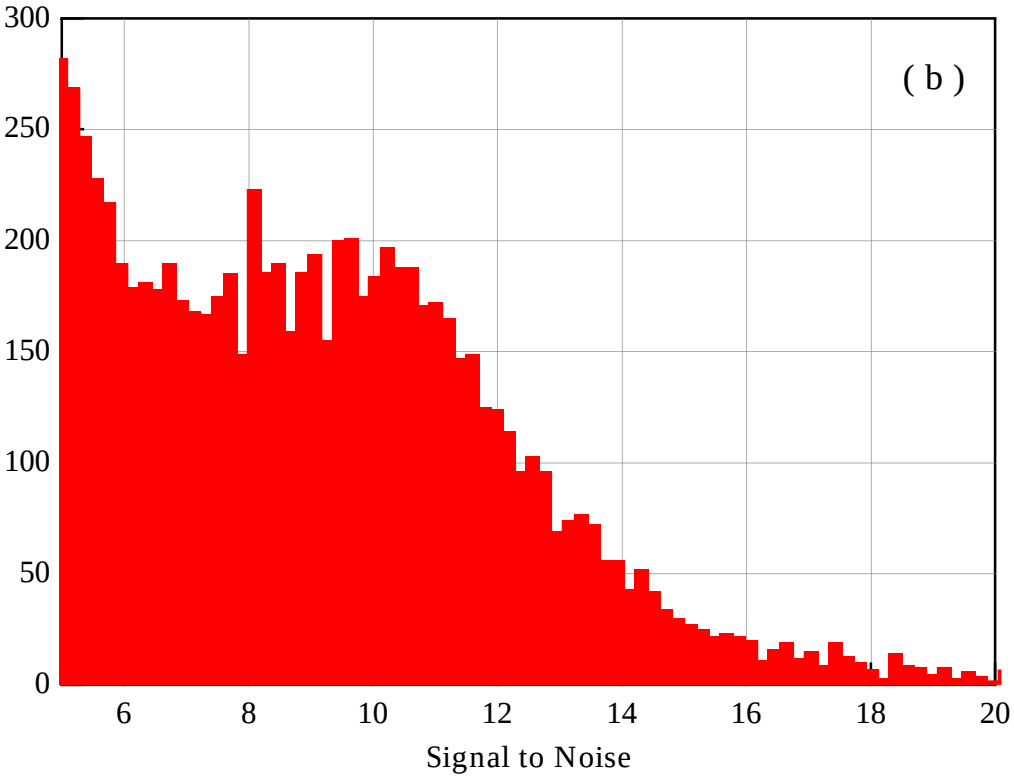

(b)
300
250
200
150
100
50
0
6
8
10
12
14
16
18
20
Signal to Noise

Figure 18

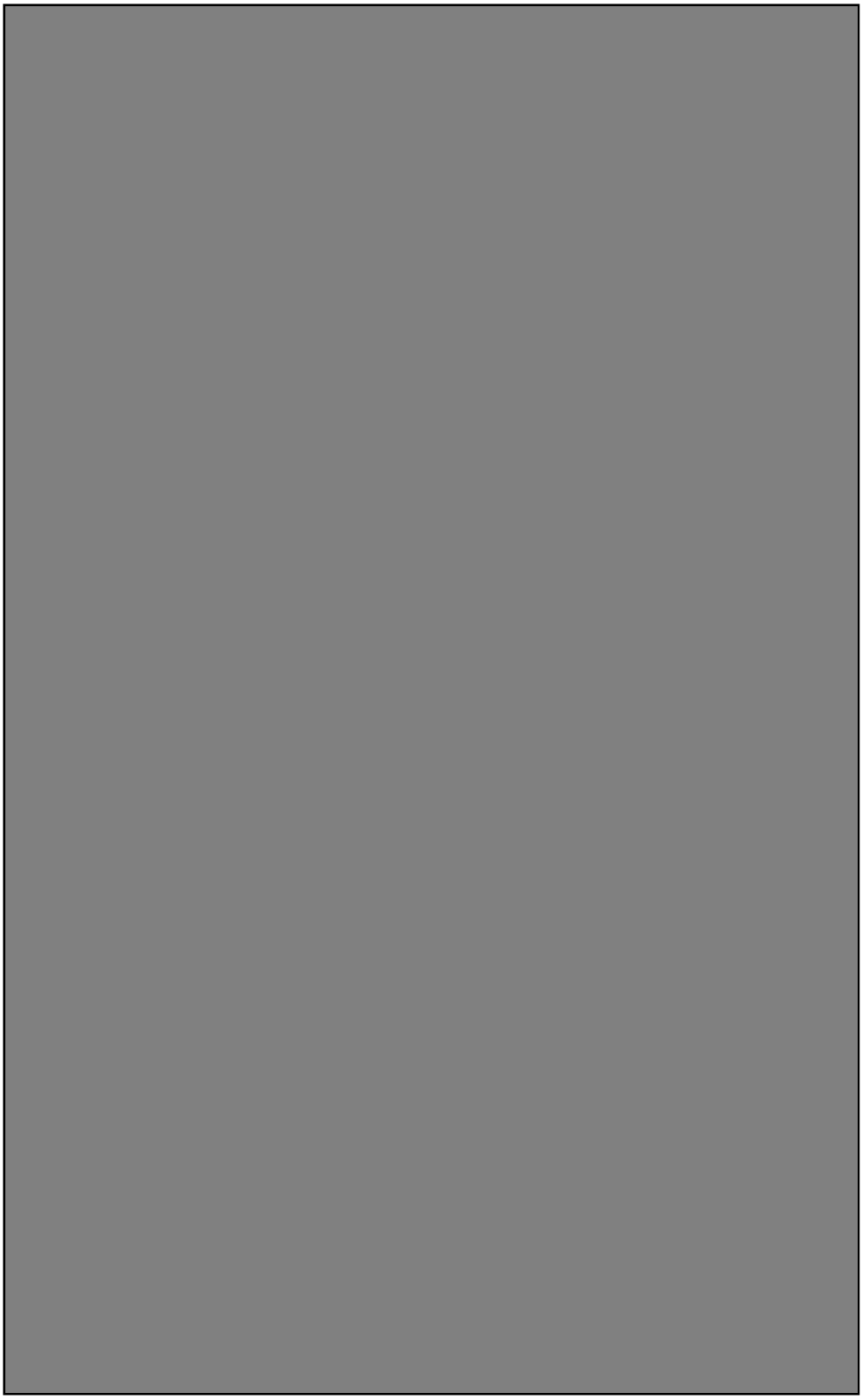


Figure 19